Remarks

The Office Action mailed August 29, 2003 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 2-5, 7-11, 13-17, 19-22, 24-26, and 28-47 are now pending in this application. Claims 1, 6, 12, 18, 23, and 27 are canceled. Claims 32-47 have been newly added. Claims 2, 3, 7, 13, 19, 24, 25, and 28 have been amended. No new matter has been added. Claims 2-5, 7-11, 13-17, 19-22, and 24-31 stand rejected.

In accordance with 37 C.F.R. 1.136(a), a two-month extension of time is submitted herewith to extend the due date of the response to the Office Action dated August 29, 2003 for the above-identified patent application from November 29, 2003 through and including January 29, 2003. In accordance with 37 C.F.R. 1.17(a)(2), authorization to charge a deposit account in the amount of $420.00 to cover this extension of time request also is submitted herewith. In addition, an authorization to charge a deposit account is submitted herewith for the newly added Claims 32-47.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under 35 U.S.C. § 112, first paragraph, is respectfully traversed. Applicants have amended Claims 2, 3, 7, 13, 19, 24, 25, and 28. Claims 4 and 5 depend on independent Claim 3, Claims 8-11 depend, directly or indirectly, from independent Claim 7, Claims 14-17 depend, directly or indirectly, from independent Claim 13, Claims 20-22 depend, directly or indirectly, from independent Claim 19, Claim 26 depends on independent Claim 25, and Claims 29-31 depend, directly or indirectly, from independent Claim 28. Accordingly, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under Section 112, first paragraph, be withdrawn.

For the reasons set forth above, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under Section 112, first paragraph, be withdrawn.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under 35 U.S.C. § 112, second paragraph, is respectfully traversed. Applicants have amended Claims 2, 3, 7, 13, 19, 24, 25, and 28. Claims 4 and 5 depend on independent Claim 3, Claims 8-11 depend, directly or indirectly, from independent Claim 7, Claims 14-17 depend, directly or indirectly, from

independent Claim 13, Claims 20-22 depend, directly or indirectly, from independent Claim 19, Claim 26 depends on independent Claim 25, and Claims 29-31 depend, directly or indirectly, from independent Claim 28. Accordingly, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under Section 112, second paragraph, be withdrawn.

For the reasons set forth above, Applicants respectfully request that the rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under Section 112, second paragraph, be withdrawn.

The rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 under 35 U.S.C. § 102(e) as being anticipated by Sagues et al. (U.S. Patent Application 2002/0119706 A1) is respectfully traversed.

Sagues et al. describe an I/O module (66) that includes a microprocessor (82) and a power supply (84) (paragraph 40). An input line (86) and output line (88) are both shown as required for Ethernet communications between the module and a controller (72) (paragraph 40). The microprocessor is also programmed/directed by the controller to cause a particular signal to be applied to any selected one or more of conductors of one or more cables such as a cable (94) (paragraph 40). The module provides a selection of interconnection devices (98-112) for each of any of a plurality of lines (94) (paragraph 41). Each set of devices (98-112) is dedicated for making a connection to one line (94) (paragraph 41).

Claim 2 recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "at least one port controlling a configuration of the at least one pin, said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port; and a comparator configured to provide an output to a processor located within said circuit."

Sagues et al. does not describe or suggest a control circuit for configuring at least one I/O module connector pin, the circuit comprising at least one port controlling a configuration of the at least one pin, the at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out

(VOUT) port, and a comparator configured to provide an output to a processor located within the circuit.

Moreover, Sagues et al. does not describe or suggest a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as recited in Claim 2. For the reasons set forth above, Claim 2 is submitted to be patentable over Sagues et al.

Claim 3 recites a control circuit for configuring at least one I/O module connector pin, the circuit comprising "at least one port controlling a configuration of the at least one pin; at least one switch assembly comprising a solid state switch, said at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state; and a comparator configured to provide an output to a processor located within said circuit."

Sagues et al. does not describe or suggest a control circuit for configuring at least one I/O module connector pin, the circuit including at least one port controlling a configuration of the at least one pin, at least one switch assembly including a solid state switch, the at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state, and a comparator configured to provide an output to a processor located within the circuit.

Moreover, Sagues et al. does not describe or suggest a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as recited in Claim 3. For the reasons set forth above, Claim 3 is submitted to be patentable over Sagues et al.

Claims 4 and 5 depend from independent Claim 3. When the recitations of Claims 4 and 5 are considered in combination with the recitations of Claim 3, Applicants submit that dependent Claims 4 and 5 likewise are patentable over Sagues et al.

Claim 7 recites an I/O module comprising "at least one connector pin; a control circuit comprising a plurality of solid state switches, said solid state switches controlling a

configuration of the at least one pin; and a comparator configured to provide an output to a processor located within said circuit."

Sagues et al. does not describe or suggest an I/O module including at least one connector pin, a control circuit including a plurality of solid state switches, the solid state switches controlling a configuration of the at least one pin, and a comparator configured to provide an output to a processor located within the circuit.

Moreover, Sagues et al. does not describe or suggest a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as recited in Claim 7. For the reasons set forth above, Claim 7 is submitted to be patentable over Sagues et al.

Claims 8-11 depend, directly or indirectly, from independent Claim 7. When the recitations of Claims 8-11 are considered in combination with the recitations of Claim 7, Applicants submit that dependent Claims 8-11 likewise are patentable over Sagues et al.

Claim 13 recites a PLC comprising "an I/O module comprising at least one connector pin and a control circuit comprising a plurality of ports, a configuration of the at least one connector pin determined by an energization state of said ports; a comparator configured to provide an output to a processor located within said circuit; and a CPU coupled to said I/O module."

Sagues et al. does not describe or suggest a PLC including an I/O module including at least one connector pin and a control circuit including a plurality of ports, a configuration of the at least one connector pin determined by an energization state of the ports, a comparator configured to provide an output to a processor located within the circuit, and a CPU coupled to the I/O module.

Moreover, Sagues et al. does not describe or suggest , a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as

recited in Claim 13. For the reasons set forth above, Claim 13 is submitted to be patentable over Sagues et al.

Claims 14-17 depend, directly or indirectly, from independent Claim 13. When the recitations of Claims 14-17 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 14-17 likewise are patentable over Sagues et al.

Claim 19 recites a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method comprising "providing an energization state to the at least one port; controlling a configuration of the at least one connector pin utilizing the energization state of the at least one port; and providing an output from a comparator to a processor located within the control circuit."

Sagues et al. does not describe or suggest a method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, the method including providing an energization state to the at least one port, controlling a configuration of the at least one connector pin utilizing the energization state of the at least one port, and providing an output from a comparator to a processor located within the control circuit.

Moreover, Sagues et al. does not describe or suggest providing an output from a comparator to a processor located within the control circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach providing an output from a comparator as recited in Claim 19. For the reasons set forth above, Claim 19 is submitted to be patentable over Sagues et al.

Claims 20-22 depend, directly or indirectly, from independent Claim 19. When the recitations of Claims 20-22 are considered in combination with the recitations of Claim 19, Applicants submit that dependent Claims 20-22 likewise are patentable over Sagues et al.

Claim 24 recites an I/O module comprising "at least one connector pin; a control circuit comprising a plurality of switches controlling a configuration of said at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of each said at least one port controlling a state of a respective at least one

switch; and a comparator configured to provide an output to a processor located within said circuit."

Sagues et al. does not describe or suggest recites an I/O module including at least one connector pin, a control circuit including a plurality of switches controlling a configuration of the at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of the at least one port controlling a state of a respective at least one switch, and a comparator configured to provide an output to a processor located within the circuit.

Moreover, Sagues et al. does not describe or suggest a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as recited in Claim 24. For the reasons set forth above, Claim 24 is submitted to be patentable over Sagues et al.

Claim 25 recites an I/O module comprising "at least one connector pin; and a control circuit comprising a plurality of switches controlling a configuration of said at least one pin, said circuit utilizing a single DAC for each said connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, a zero to ten volt analog input mode, and a zero to ten volt analog output mode; and a comparator configured to provide an output to a processor located within said circuit."

Sagues et al. does not describe or suggest an I/O module including at least one connector pin, and a control circuit including a plurality of switches controlling a configuration of the at least one pin, the circuit utilizing a single DAC for each connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt

low side discrete output mode with open wire detection, a zero to ten volt analog input mode, and a zero to ten volt analog output mode; and a comparator configured to provide an output to a processor located within the circuit.

Moreover, Sagues et al. does not describe or suggest a comparator configured to provide an output to a processor located within the circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. do not teach the comparator as recited in Claim 25. For the reasons set forth above, Claim 25 is submitted to be patentable over Sagues et al.

Claims 26 depends from independent Claim 25. When the recitations of Claim 26 are considered in combination with the recitations of Claim 25, Applicants submit that dependent Claim 26 likewise is patentable over Sagues et al.

Claim 28 recites a method for configuring at least one connector pin utilizing a control circuit, the method comprising "controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, zero to ten volt analog input mode, and a zero to ten volt analog output mode; and providing an output from a comparator to a processor located within the control circuit."

Sagues et al. does not describe or suggest a method for configuring at least one connector pin utilizing a control circuit, the method including controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, a zero to ten volt analog input

mode, and a zero to ten volt analog output mode, and providing an output from a comparator to a processor located within the control circuit.

Moreover, Sagues et al. does not describe or suggest providing an output from a comparator to a processor located within the control circuit. Rather, Sagues et al. describe the I/O module that includes a microprocessor, a power supply, and a set of devices dedicated for making a connection to one line. Accordingly, Sagues et al. does not teach providing an output from a comparator as recited in Claim 28. For the reasons set forth above, Claim 28 is submitted to be patentable over Sagues et al.

Claims 29-31 depend, directly or indirectly, from independent Claim 28. When the recitations of Claims 29-31 are considered in combination with the recitations of Claim 28, Applicants submit that dependent Claims 29-31 likewise are patentable over Sagues et al.

For the reasons set forth above, Applicants respectfully request that the Section 102 rejection of Claims 2-5, 7-11, 13-17, 19-22, and 24-31 be withdrawn.

Newly added Claims 32-33 depend, directly or indirectly, from independent Claim 2, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 32-33 are also patentable over the cited art.

Newly added Claims 34-35 depend, directly or indirectly, from independent Claim 3, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 34-35 are also patentable over the cited art.

Newly added Claims 36-37 depend, directly or indirectly, from independent Claim 7, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 36-37 are also patentable over the cited art.

Newly added Claims 38-39 depend, directly or indirectly, from independent Claim 13, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 38-39 are also patentable over the cited art.

Newly added Claims 40-41 depend, directly or indirectly, from independent Claim 19, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 40-41 are also patentable over the cited art.

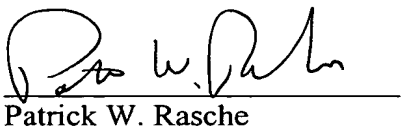
Newly added Claims 42-43 depend, directly or indirectly, from independent Claim 24, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 42-43 are also patentable over the cited art.

Newly added Claims 44-45 depend, directly or indirectly, from independent Claim 25, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 44-45 are also patentable over the cited art.

Newly added Claims 46-47 depend, directly or indirectly, from independent Claim 28, which is submitted to be in condition for allowance and patentable over the cited art. For at least the reasons set forth above, Applicants respectfully submit that Claims 46-47 are also patentable over the cited art.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



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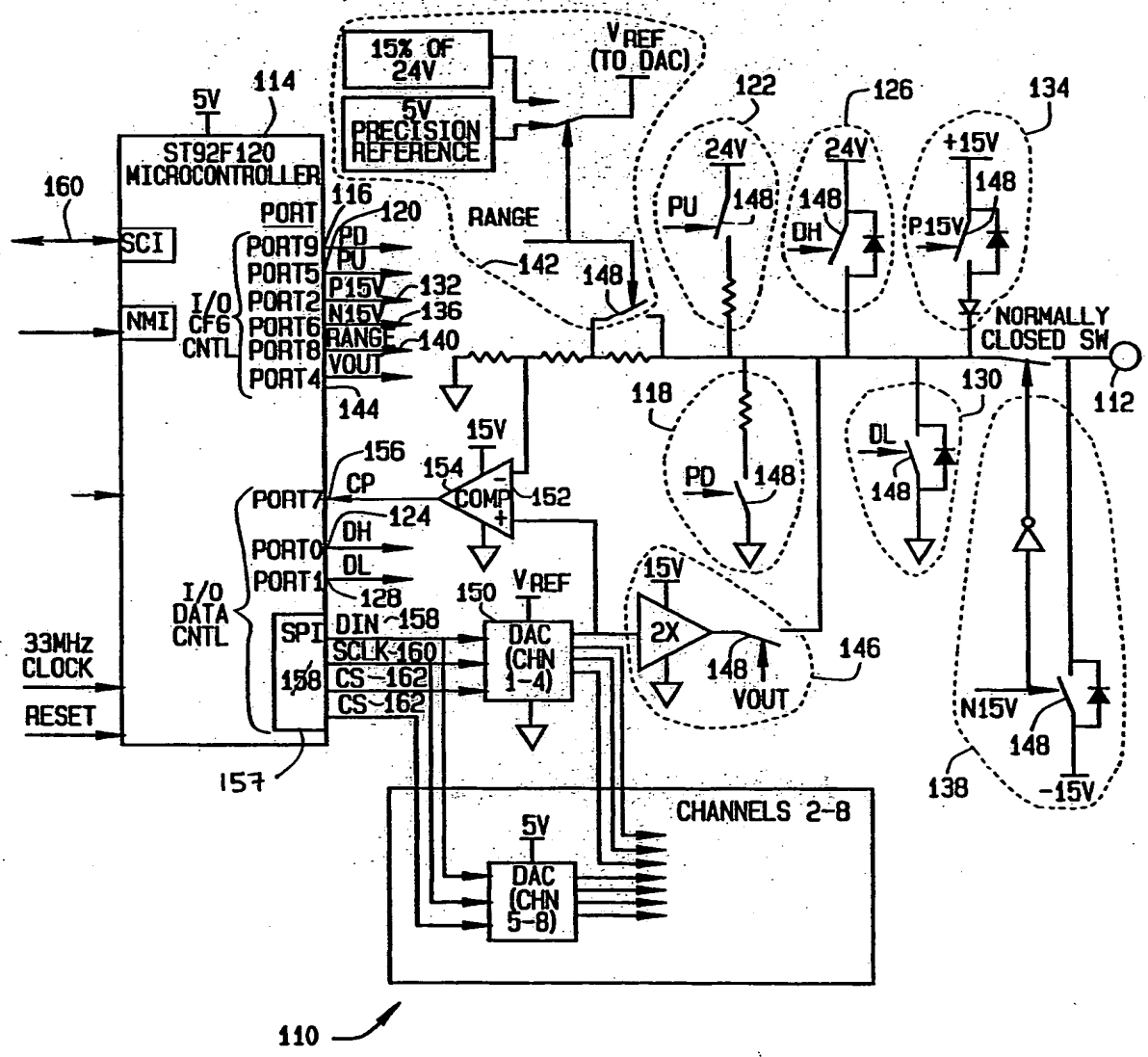

FIG. 3